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(71) Applicant: **MATSUSHITA ELECTRON CORP**

(72) Inventor: **SHIMAKAWA KAZUHIKO**

(54) **NONVOLATILE STORAGE**

(57) Abstract:

PURPOSE: To reduce potential variation at the time when a non-selective bit line is selected, and to execute the read-out operation at a high speed by connecting the non-selective bit line and a source of a cell transistor corresponding to its bit line to the bit line potential by a potential setting means.

CONSTITUTION: In accordance with an address input, one piece of four pieces of word lines W_1 - W_4 is selected and set to a high level, and a transistor of the line becomes a turn-on state. Also, one piece of four pieces of bit lines and a source line selecting line is set to a high level, a bit line of the row is set to a connecting state to a sense amplifier, and a source line is connected electrically to a ground level. On the other hand, in four pieces of non-selective bit lines and non-selective source line selecting signal lines the inverse of C_1,... the inverse of C_4 of a potential setting means 3, three pieces are set to a high level so that other non-selective bit line and non-selective source line than the selective bit line and the source line are selected, and connected electrically to a bit line potential generating circuit

1. In such a way, the read-out operation can be executed at a high speed.